CLAIMS

1. A preamplifier circuit, comprising:

first and second input ports;

the first input port configured to receive a first signal which includes a read sensor data signal and an interference signal;

the second input port configured to receive a second signal which includes the interference signal but not the read sensor data signal; and

a subtractor having first and second inputs coupled to the first and the second input ports, respectively.

2. The preamplifier circuit of claim 1, further comprising:

an output of the subtractor which provides the read sensor signal substantially without the interference signal.

3. The preamplifier circuit of claim 1, wherein the preamplifier circuit is embodied in an integrated circuit (IC).

4. The preamplifier circuit of claim 1, further comprising:

a first bias source which provides a first read sensor current/voltage bias at the first input port; and

a second bias source which provides a second read sensor current/voltage bias at the second input port.

5. The preamplifier circuit of claim 1, further comprising:

a first bias source which provides a first read sensor current/voltage bias at the first input port;

a second bias source which provides a second read sensor current/voltage bias at the second input port; and

wherein the second bias is set to zero or is negligible.

6. The preamplifier circuit of claim 1, further comprising:

a first amplifier having an input coupled to the first input port and an output coupled to the first input of the subtractor; and

a second amplifier having an input coupled to the second input port and an output coupled to the second input of the subtractor.

7. The preamplifier circuit of claim 1, further comprising:

a first bias source which provides a first read sensor current/voltage bias at the first input port;

a second bias source which provides a second read sensor current/voltage bias at the second input port;

wherein the second read sensor bias is set to zero or is negligible;

a first amplifier having an input coupled to the first input port and an output coupled to the first input of the subtractor; and

a second amplifier having an input coupled to the second input port and an output coupled to the second input of the subtractor.

8. The preamplifier circuit of claim 1, further comprising:

a first bias source which provides a first read sensor current/voltage bias at the first input port;

a second bias source which provides a second read sensor current/voltage bias at the second input port;

wherein the second read sensor bias is set to zero or is negligible;

a first amplifier having an input coupled to the first input port and an output coupled to the first input of the subtractor;

a second amplifier having an input coupled to the second input port and an output coupled to the second input of the subtractor; and

wherein a gain of at least one of the first and the second amplifiers is controllably adjusted so that an output of the subtractor provides the read sensor signal substantially without the interference signal.

9. The preamplifier circuit of claim 1, further comprising:

a first bias source which provides a first read sensor current/voltage bias at the first input port;

a second bias source which provides a second read sensor current/voltage bias at the second input port;

a first amplifier which includes a first transistor having a base coupled to the first input port, a collector coupled to a first reference voltage through a first resistor, and an emitter coupled to a second reference voltage; and

a second amplifier which includes a second transistor having a base coupled to the second input port, a collector coupled to the first reference voltage through a second resistor, and an emitter coupled to the second reference voltage.

10. The preamplifier circuit of claim 1, further comprising:

a first amplifier which includes a first transistor having a base coupled to the first input port through a first capacitor, a collector coupled to a first reference voltage through a first resistor, and an emitter coupled to a second reference voltage;

a second amplifier which includes a second transistor having a base coupled to the second input port through a second capacitor, a collector coupled to the first reference voltage through a second resistor, and an emitter coupled to the second reference voltage;

a first bias source which provides a first read sensor current/voltage bias at the first input port;

a second bias source which provides a second read sensor current/voltage bias at the second input port; and

wherein the second bias source is set to zero or is negligible.

11. The preamplifier circuit of claim 1, further comprising:

a first amplifier which includes a first transistor having a base coupled to the first input port through a first capacitor, a collector coupled to a first reference voltage through a first resistor, and an emitter coupled to a second reference voltage;

a second amplifier which includes a second transistor having a base coupled to the second input port through a second capacitor, a collector coupled to the first reference voltage through a second resistor, and an emitter coupled to the second reference voltage;

a second amplifier which includes a second transistor having a base coupled to the second input port through a second capacitor, a collector coupled to the first reference voltage through a second resistor, and an emitter coupled to the second reference voltage;

a second amplifier which includes a second transistor having a base coupled to the second input port through a second capacitor, a collector coupled to the first reference voltage through a second resistor, and an emitter coupled to the second reference voltage;

a first bias source which provides a first read sensor current/voltage bias at the first input port;

a second bias source which provides a second read sensor current/voltage bias at the second input port; and

wherein the second bias source is set to zero or is negligible.

12. A preamplifier circuit, comprising:

first and second input ports;

the first input port being configured to receive a first signal which includes an input signal and an interference signal;

the second input port being configured to receive a second signal which includes the interference signal but not the input signal; and

a subtractor having first and second inputs coupled to the first and the second input ports, respectively.

13. The preamplifier circuit of claim 12, further comprising:

a first bias source which provides a first current/voltage bias at the first input port;

a second bias source which provides a second current/voltage bias at the second input port; and

wherein the second bias is set to zero or is negligible.

14. The preamplifier circuit of claim 12, further comprising:

a first amplifier having an input coupled to the first input port and an output coupled to the first input of the subtractor; and

a second amplifier having an input coupled to the second input port and an output coupled to the second input of the subtractor.

15. The preamplifier circuit of claim 12, further comprising:

a first bias source which provides a first current/voltage bias at the first input port;

a second bias source which provides a second current/voltage bias at the second input port;

wherein the second read sensor bias is set to zero or is negligible;

a first amplifier having an input coupled to the first input port and an output coupled to the first input of the subtractor; and

a second amplifier having an input coupled to the second input port and an output coupled to the second input of the subtractor.

16. The preamplifier circuit of claim 12, further comprising:

a first bias source which provides a first current/voltage bias at the first input port;

a second bias source which provides a second current/voltage bias at the second input port;

wherein the second read sensor bias is set to zero or is negligible;

a first amplifier having an input coupled to the first input port and an output coupled to the first input of the subtractor;

a second amplifier having an input coupled to the second input port and an output coupled to the second input of the subtractor; and

wherein a gain of at least one of the first and the second amplifiers is controllably adjusted so that an output of the subtractor provides the input signal substantially without the interference signal.

17. The preamplifier circuit of claim 12, further comprising:

a first bias source which provides a first current/voltage bias at the first input port;

a second bias source which provides a second current/voltage bias at the second input port;

a first amplifier which includes a first transistor having a base coupled to the first input port, a collector coupled to a first reference voltage through a first resistor, and an emitter coupled to a second reference voltage; and

a second amplifier which includes a second transistor having a base coupled to the second input port, a collector coupled to the first reference voltage through a second resistor, and an emitter coupled to the second reference voltage.

18. The preamplifier circuit of claim 12, further comprising:

a first amplifier which includes a first transistor having a base coupled to the first input port through a first capacitor, a collector coupled to a first reference voltage through a first resistor, and an emitter coupled to a second reference voltage;

a second amplifier which includes a second transistor having a base coupled to the second input port through a second capacitor, a collector coupled to the first reference voltage through a second resistor, and an emitter coupled to the second reference voltage;

a first bias source which provides a first current/voltage bias at the first input port;

a second bias source which provides a second current/voltage bias at the second input port; and

wherein the second bias source is set to zero or is negligible.

19. The preamplifier circuit of claim 12, further comprising:

a first amplifier which includes a first transistor having a base coupled to the first input port through a first capacitor, a collector coupled to a first reference voltage through a first resistor, and an emitter coupled to a second reference voltage;

a second amplifier which includes a second transistor having a base coupled to the second input port through a second capacitor, a collector coupled to the first reference voltage through a second resistor, and an emitter coupled to the second reference voltage;

a third amplifier which includes a third transistor having a base coupled to the collector of the first transistor, a collector coupled to the first reference voltage through a third resistor, and an emitter coupled to the second reference voltage;

a fourth amplifier which includes a fourth transistor having a base coupled to the collector of the second transistor, a collector coupled to the first reference voltage through a fourth resistor, and an emitter coupled to the second reference voltage;

a first bias source which provides a first current/voltage bias at the first input port;

a second bias source which provides a second current/voltage bias at the second input port; and

wherein the second bias source is set to zero or is negligible.

20. A magnetic storage device, comprising:

at least one magnetic disk;

a magnetic head which includes first and second read sensors;

a suspension which supports the magnetic head relative to the magnetic disk;

read circuitry having a preamplifier which includes:

a first input port coupled to the first read sensor;

a second input port coupled to the second read sensor;

a subtractor having first and second inputs coupled to the first and the second input ports, respectively; and

an output of the subtractor which provides a read sensor data signal.

21. The magnetic storage device of claim 20, wherein the preamplifier is embodied in an integrated circuit (IC).

22. The magnetic storage device of claim 20, further comprising:

a first bias source coupled to the first input port of the preamplifier; and

a second bias source coupled to the second input port of the preamplifier.

23. The magnetic storage device of claim 20, further comprising:

a first bias source coupled to the first input port of the preamplifier;

a second bias source coupled to the second input port of the preamplifier; and

wherein the second bias source is configured to provide a zero or negligible bias.

24. The magnetic storage device of claim 20, further comprising:

a first bias source coupled to the first input port of the preamplifier;

a second bias source coupled to the second input port of the preamplifier;

wherein the second bias source is set to provide a zero or negligible bias for the second read sensor;

a first amplifier coupled between the first input port and the first input of the subtractor; and

a second amplifier coupled between the second input port and the second input of the subtractor.

25. The magnetic storage device of claim 20, further comprising:

a first bias source coupled to the first input port of the preamplifier;

a second bias source coupled to the second input port of the preamplifier;

wherein the second bias source is set to provide a zero or negligible bias for the second read sensor;

a first amplifier coupled between the first input port and the first input of the subtractor;

a second amplifier coupled between the second input port and the second input of the subtractor; and

wherein a gain of at least one of the first and the second amplifiers is controllably adjusted so that an output of the subtractor provides the input signal substantially without an interference signal.

26. In a preamplifier circuit, a method of reducing interference in a read sensor signal comprising:

receiving a first signal which includes a read sensor data signal and an interference signal;

receiving a second signal which includes the interference signal but not the read sensor data signal; and

subtracting the second signal from the first signal to provide a read sensor signal without the interference signal.

27. The method of claim 26, further comprising:

wherein the first signal is from a first read sensor; and

wherein the second signal is from a second read sensor.

28. The method of claim 26, further comprising:

providing an active current/voltage bias for a first read sensor to receive the first signal; and

providing a zero current/voltage bias for a second read sensor to receive the second signal.

29. The method of claim 26, further comprising:

amplifying the read sensor data signal after subtracting the second signal from the first signal.

30. The method of claim 26, further comprising:

providing an active current/voltage bias for a first read sensor to receive the first signal;

providing a zero current/voltage bias for a second read sensor to receive the second signal; and

amplifying the read sensor data signal after subtracting the second signal from the first signal.